TITLE	DOC No. RFD-20260926004-002	
800G QSFP-DD 2xDR4 500m Transceivers	REVISION : 01	AUTHORIZED BY : Hawk Rong
	DATE : 2026.07.06	CLASSIFICATION : Optical Transceivers

1. Product Features

- Compliant with IEEE 802.3cu-2021:
- 8x100GBASE-DR optical interface
- Compliant with IEEE 802.3ck-2022:
- 8x100GAUI-1 C2M electrical interface
- Compliant with QSFP-DD MSA HW Rev 7.0 type 2B with Dual MPO-12 connector
- Compliant with CMIS Rev 5.0
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

2. Product Description

Product Name And Series Number(s)

800G QSFP-DD 2xDR4 500m Transceivers

JPC P/N	Laser	Distance	Power	Sen	Connector	Temp.
P66**0KRCBS5-1	1311nm	500m	-2.9~4dBm	≥–3.9dBm	Dual MPO12	C

Note-1： ** **Indicates the customer code.**

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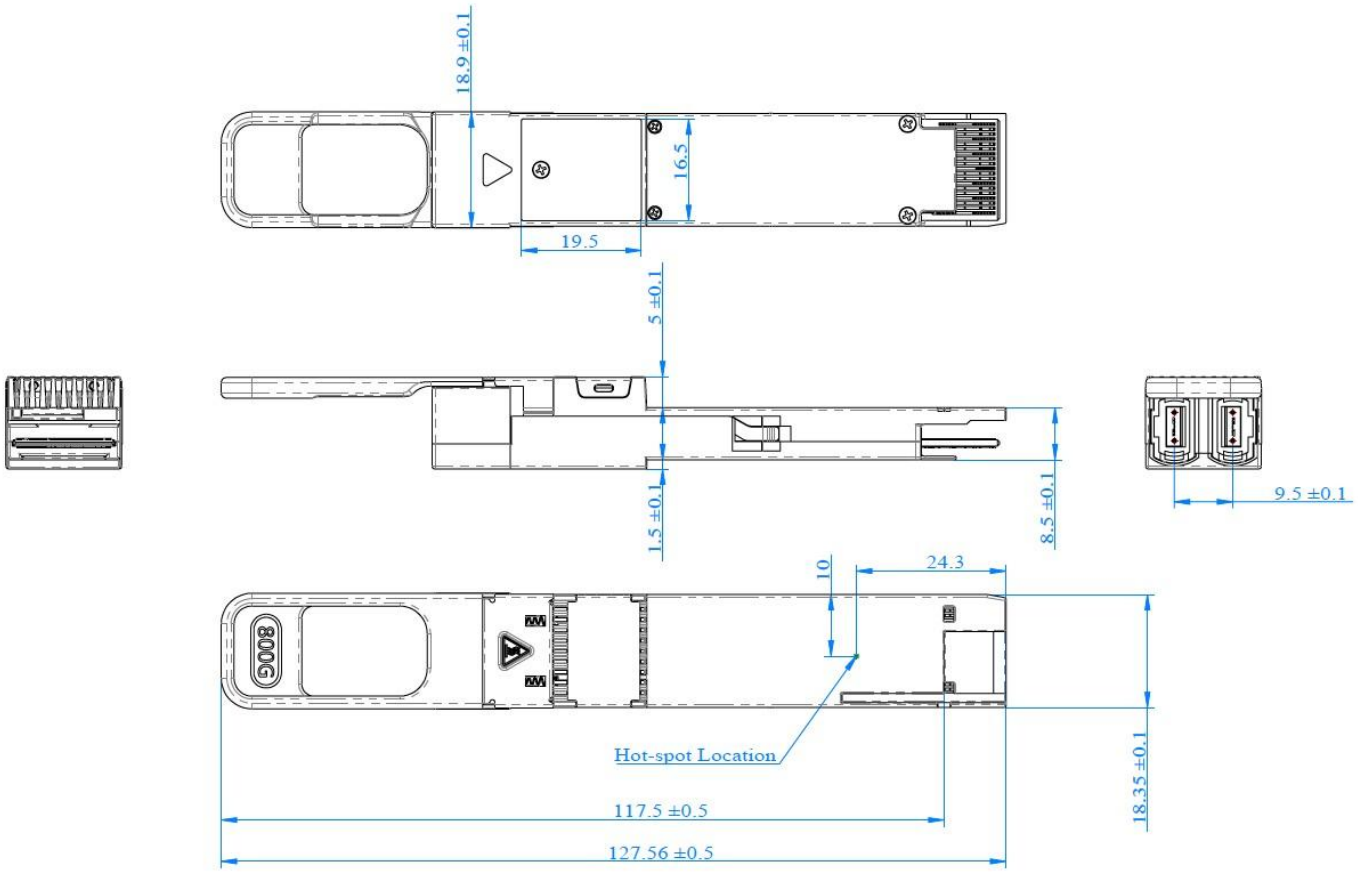
2.1 Dimensions,Materials,Platings And Marking



Unit is millimeter. All dimensions are ±0.1mm unless otherwise specified

3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	TS	-40	85	ºC	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	IVDIP-VDINI	-	1	V	

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Control Input Voltage	VI	-0.3	VCC+0.5	V	
Control Output Current	IO	-20	20	mA	

4. Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0	-	70	ºC	1
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP	-	-	6600	mA	
Sustained peak current at hot plug	ICC_SP	-	-	5446	mA	
Maximum Power Dissipation	PD	-	-	16.5	W	
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	2	W	
Signalling Speed per Lane	DRL	-	53.125	-	GBd	
Control Input Voltage High	VIH	VCC*0.7	-	VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3	-	VCC*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)	-	-	-	66	mVpp	
Operating Distance	-	2	-	500	m	

5. Transmitter Optical Specification

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λC	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each lane	AOPL	-2.9	-	4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter),	TOMA	-0.8	-	4.2	dBm	

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each Lane						
Launch power in OMAouter minus TDECQ, each lane for extinction ratio >= 5 dB for extinction ratio < 5 dB	TOMA-TDECQ	-2.2 -1.9	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
TDECQ – 10log10(Ceq), each lane	Ceq	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-15	dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Transmitter transition time	Tr			17	ps	
RIN15.5OMA	RIN	-	-	-136	dB/Hz	
Optical return loss tolerance	ORL	-	-	15.5	dB	
Transmitter Reflectance	TR	-	-	-26	dB	2

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength

Note 2: Transmitter reflectance is defined looking into the transmitter.

6. Receiver Optical Specification

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λC0	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOPD	5	-	-	dBm	
Average Receive Power, each Lane	AOPR	-5.9	-	4	dBm	
Receive Power (OMAouter), each Lane	OMAR	-	-	4.2	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMAouter), each Lane	SOMA	-	-	Max(–3.9, SECQ – 5.3)	dBm	1

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Stressed Receiver Sensitivity (OMAouter), each Lane	SRS	-	-	-1.9	dBm	2
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	-	3.4	-	dB	
SECQ – 10log10(Ceq), lane under test	Ceq	-	-	3.4	dB	
OMAouter of each aggressor lane	-	-	4.2	-	dBm	

Note 1: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQup to 3.4 dB.
Note 2: Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$

7. Electrical Specification High Speed Signal

Receiver (Module Output, TP4)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB	-	-	-	32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode	-	-	-	600 845	mV	
Eye height	EH	15	-	-	mV	
Vertical eye closure	VEC	-	-	12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Transition time	-	8.5	-	-	ps	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	
Transmitter (Module Input, TP1)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential pk-pk input Voltage tolerance	-	750	-	-	mV	

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(TP1a)						
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB	-	32 80	-	-	mV	
Differential-mode to common-mode return loss	RLcd	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5	-	-	dB	
Differential termination mismatch	-	-	-	10	%	
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	
DC common-mode voltage tolerance	-	-0.35	-	2.85	V	

8. Electrical Specification Low Speed Control and Sense Signals

Parameter	Symbol	Min.	Max.	Unit	Condition
Module output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

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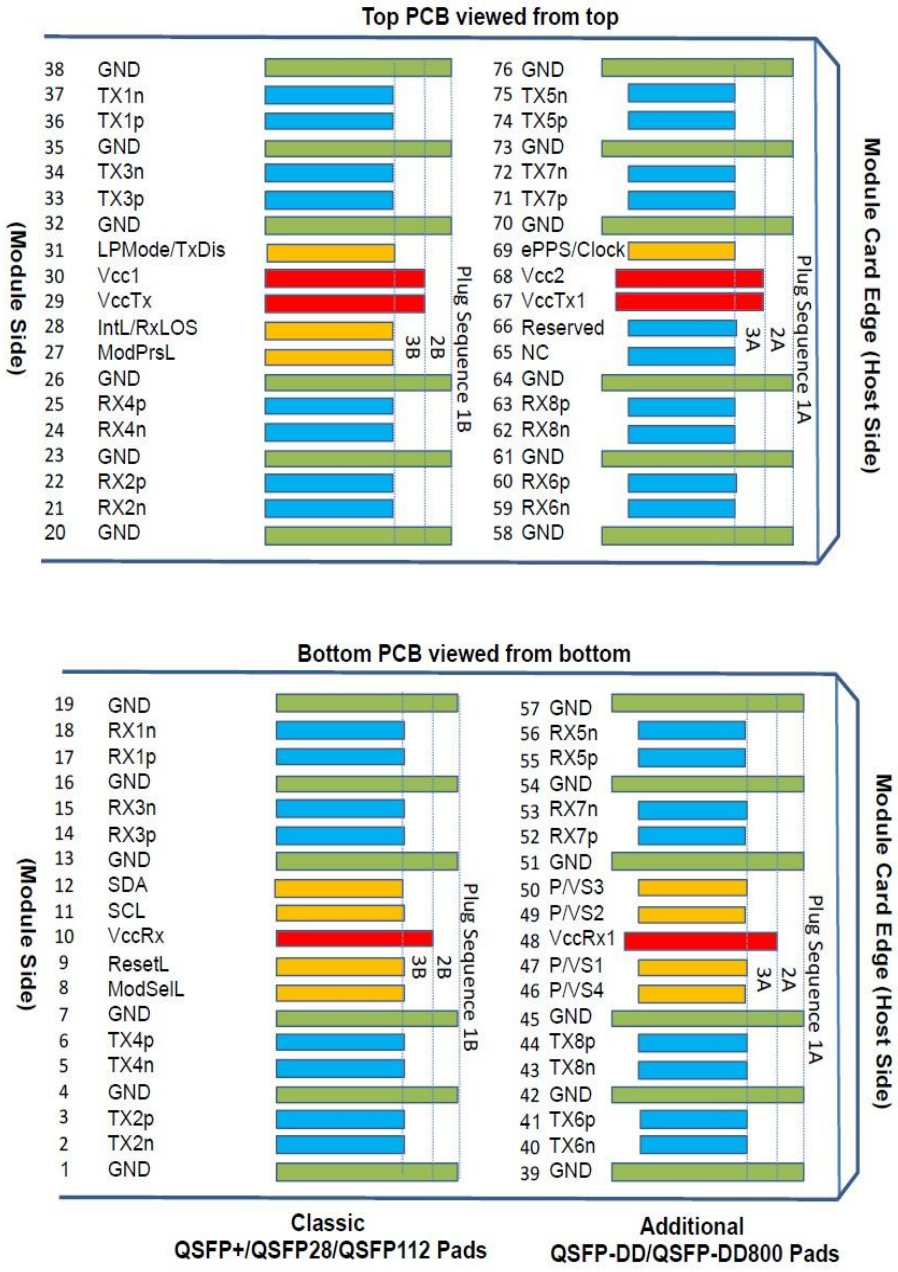
9. Applications Note:

Pin Definitions



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Pin Function Definitions

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4
9	LVTTL-I	ResetL	Module Reset	47	LVCMOS /CML-I	P/VS1	Programmable/Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	TWI serial interface clock	49	LVCMOS /CML-O	P/VS2	Programmable/Module Vendor Specific 2
12	LVCMOS-I/O	SDA	TWI serial interface data	50	LVCMOS /CML-O	P/VS3	Programmable/Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output

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16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	LPMode/ TxDis	Low Power mode/optional TX Disable	69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input

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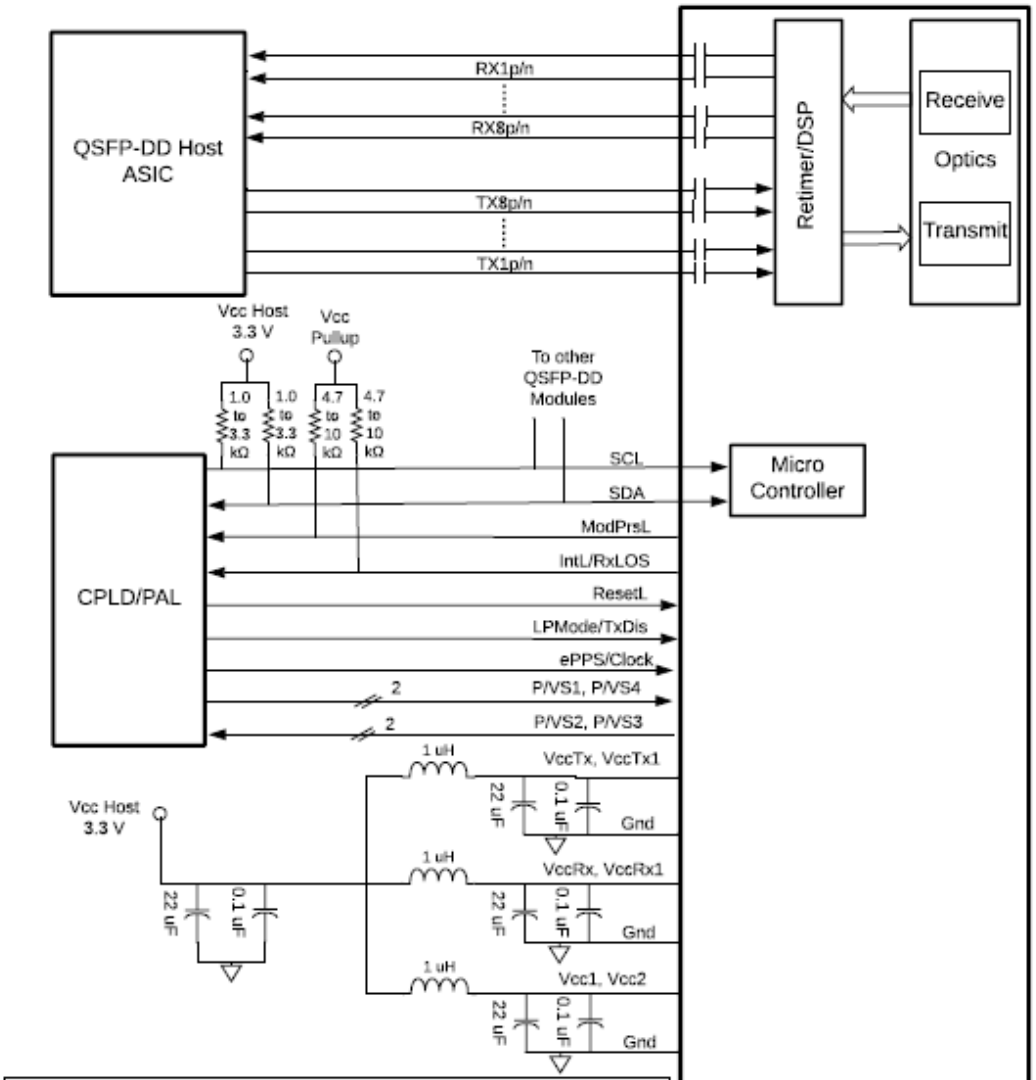
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

10. Recommended QSFP-DD/QSFP-DD800 Host Board Schematic



Note: Filter capacitors values are informative and application dependent, 0.1 µF capacitors should be placed in close proximity to power pads and may be duplicated for individual pads to provide additional high frequency filtering.

Note: Vcc1/Vcc2 may be connected to VccTx/VccTx1 or VccRx/VccRx1 within the module provided the applicable derating of the maximum current limit is used.

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11. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	3.135 to 3.465	±3%	V	Internal
Tx Bias Current (Each Lane)	0 to 15	10%	mA	Internal
Tx Output Power (Each Lane)	-4.6 to +4	±3	dB	Internal
Rx Receive Power (Each Lane)	-6.3 to +4	±3	dB	Internal

12. Modification History

Rev.	Comments	Date	Originator	Approval
01	Initial	2026.07.06	Hawk Rong	Mike Sun